CLAIMS

I claim:

1. A high-voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a well region of a second conductivity type, opposite to the first conductivity type, disposed in the substrate;

a source diffusion region of the first conductivity type disposed in the N-well region;

a first drain diffusion region of the first conductivity type disposed in the N-well region spaced-apart from the source diffusion region, a channel region being defined in the well region between the source diffusion region and the first drain diffusion region;

a second drain diffusion region of the first conductivity type disposed in the well region spaced-apart from the first drain diffusion region;

a buried layer region of the first conductivity type disposed within the well region, extending laterally from beneath the first drain diffusion region to beneath the second drain diffusion region, the buried layer region being connected to both the first and second P-type drain diffusion regions such that current flows laterally through the buried layer region when the HVFET is in an on-state; and

an insulated gate formed over the channel region.

2. The HVFET according to claim 1 further comprising:

a source electrode connected to the source diffusion region; and

a drain electrode connected to the second drain diffusion region.

3. The HVFET according to claim 2 further comprising:

a diffusion region of the second conductivity type disposed in the well region adjacent the source diffusion region, the diffusion region being connected to the source electrode.

4. The HVFET according to claim 2 wherein the first conductivity type is P-type and the second conductivity type is N-type, and the second drain diffusion region comprises:

a P+ diffusion region connected to the drain electrode; and

an additional P-type diffusion region that extends from the P+ diffusion region to the buried layer region.

5. The HVFET according to claim 2 wherein the source and drain electrodes each comprise laterally extended portions that function as field plates.

6. The HVFET according to claim 5 further comprising a drain field plate member disposed adjacent to and insulated from the second drain diffusion region, the drain field plate member also being disposed beneath and insulated from the laterally extended portion of the drain electrode.

7. The HVFET according to claim 1 wherein the buried layer region comprises a plurality of buried layers.

8. The HVFET according to claim 7 wherein the first drain diffusion region extends vertically in the well region to connect to each of the plurality of buried layers.

9. The HVFET according to claim 8 wherein the second drain diffusion region extends vertically in the well region to connect to each of the plurality of buried layers.

10. The HVFET according to claim 1 wherein the first drain diffusion region has a first surface that adjoins a surface of the substrate.

11. The HVFET according to claim 1 wherein the first conductivity type is N-type and the second conductivity type is P-type.

12. The HVFET according to claim 1 wherein the first drain diffusion region is depleted at a relatively low voltage.

13. A high-voltage field-effect transistor (HVFET) comprising:

a substrate of a first conductivity type;

a well region of a second conductivity type opposite to the first conductivity type, the well region being disposed in the substrate;

a source diffusion region of the first conductivity type disposed in the well region;

a first drain diffusion region of the first conductivity type disposed in the well region laterally spaced-apart from the source diffusion region;

a second drain diffusion region of the first conductivity type disposed in the well between the first drain diffusion region and the source diffusion region, a channel region being defined in the well region between the source diffusion region and the second drain diffusion region;

a plurality of parallel, spaced-apart buried layers of the first conductivity type disposed within the well region, the buried layers extending laterally from beneath the first drain diffusion region to beneath the second drain diffusion region, the first and second drain diffusion regions extending vertically in the well region to connect to each of the buried layers such that current flows laterally through each of the buried layers when the HVFET is in an on-state; and

an insulated gate formed over the channel region.

14. The HVFET according to claim 13 further comprising:

a source electrode connected to the source diffusion region; and

a drain electrode connected to the first drain diffusion region.

15. The HVFET according to claim 14 further comprising:

a diffusion region of the second conductivity type disposed in the well region adjacent the source diffusion region, the diffusion region being connected to the source electrode.

16. The HVFET according to claim 14 the first conductivity type is P-type and the second conductivity type is N-type, and the first drain diffusion region comprises:

a P+ diffusion region connected to the drain electrode; and

an additional P-type diffusion region that vertically extends down from the P+ diffusion region to each of the buried layers.

17. The HVFET according to claim 14 wherein the source and drain electrodes each comprise laterally extended portions that function as field plates.

18. The HVFET according to claim 17 further comprising a drain field plate member disposed adjacent to and insulated from the first drain diffusion region, the drain field plate member also being disposed beneath and insulated from the laterally extended portion of the drain electrode.

19. The HVFET according to claim 13 wherein each of the buried layers are fully depleted at a relatively low voltage when the HVFET is in an off-state.

20. The HVFET according to claim 14 wherein the first drain diffusion region comprises a diffusion region that contacts the drain electrode and extends vertically down in the well region to connect with each of the of buried layers.

21. The HVFET according to claim 13 wherein the second drain diffusion region has a first surface that adjoins a surface of the substrate.

22. The HVFET according to claim 13 wherein the first conductivity type is N-type and the second conductivity type is P-type.

23. A method of fabricating a high-voltage field-effect transistor (HVFET) in a substrate of a first conductivity type comprising:

forming a well of a second conductivity type opposite to the first conductivity type in the substrate;

implanting a dopant of the first conductivity type into the well to form a laterally extended buried layer region of the first conductivity type within the well;

forming an insulated gate above the well;

forming a first drain region of the first conductivity type and a source region of the first conductivity type spaced-apart in the well region;

forming a second drain region of the first conductivity type spaced-apart from the first drain region and located between the first drain region and the source region, a channel region being defined in the well between the source region and the second drain region under the insulated gate; and

wherein the first and second drain regions extend vertically down through the well to connect with the buried layer region so that the buried layer region provides a conductivity path for current to flow laterally when the HVFET is in an on-state.

24. The method according to claim 23 wherein the first conductivity type is P-type and the dopant comprises boron.

25. The method according to claim 23 wherein the buried layer region comprises a plurality of parallel, spaced-apart buried layers disposed at different depths within the well.

26. The method according to claim 23 wherein implanting the dopant to form the buried layer region within the well also forms another buried layer region of the first conductivity type for a complementary HVFET also disposed in the substrate.

27. The method according to claim 23 further comprising:

forming a source electrode connected to the first drain region; and

forming a drain electrode connected to the source region.

28. The method according to claim 24 wherein the first conductivity type is P-type and the second conductivity type is N-type, and forming the first drain region further comprises:

forming a P+ region connected to the drain electrode; and

forming an additional P-type region that extends from the P+ region down to the buried layer region.

29. A method of fabricating complementary high-voltage field-effect transistors (HVFETs) in a substrate of a first conductivity type comprising:

forming first and second well regions of a second conductivity type opposite to the first conductivity type in the substrate;

implanting a dopant of the first conductivity type into the first and second well regions to form first and second laterally extended buried layer regions within the first and second well regions, respectively;

forming a first insulated gate above the first well region, and a second insulated gate above the substrate adjacent the second well region;

forming a first drain region and a first source region of the first conductivity type spaced-apart in the first well region, the first drain and source regions being associated with a first HVFET;

forming an additional drain region of the first conductivity type in the first well region spaced-apart from the first drain region and located between the first drain region and the first source region, a first channel region being defined in the first well region between the first source region and the additional drain region under the first insulated gate;

forming a second drain region of the second conductivity type in the second well region, and a second source region of the second conductivity type spaced-

apart from the second well region, the second drain and source regions being associated with a second HVFET, a second channel region being defined between the second source region and the second well region under the second insulated gate;

wherein the first and additional drain regions extend vertically down through the first well region to connect with the first laterally extended buried layer region so that the first laterally extended buried layer region provides a conductivity path for current to flow laterally when the first HVFET is in an on-state, the second laterally extended buried layer region defining corresponding JFET conduction paths in the second well when the second HVFET is in an on-state.

30. The method according to claim 29 wherein the first conductivity type is P-type and the dopant comprises boron.

31. The method according to claim 29 wherein the first and second laterally extended buried layer regions each comprise a plurality of parallel, spaced-apart buried layers disposed at different depths within the first and second well regions.

32. The method according to claim 29 wherein the first and second laterally extended buried layer regions are formed simultaneously by implantation.